

**Digital Logic Lab Assignment # 9**

* To design BCD to excess 3 code converter

**Submitted By**

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Year I / SEM I

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**OBJECTIVE 10.1: To design 3-bit ODD parity generator:**

**THEORY:**

A Parity Generator is a Combinational Logic Circuit that Generates the Parity bit in the Transmitter. A Parity bit is used for the Purpose of Detecting Errors during Transmissions of binary Information. The total number of bits must be odd in order to generate the odd parity bit.

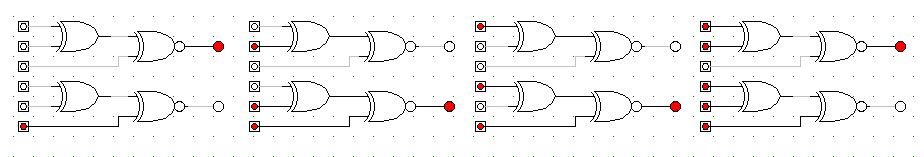
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **3 bit message** | | | 3 Bit Parity Generated |
| **X** | **Y** | **Z** | **P** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**OBSERVATIONS:**



**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **3 bit message** | | | 3 Bit Parity Generated |
| **X** | **Y** | **Z** | **P** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**CONCLUSION:**

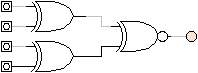
Hence, 3-bit odd parity generator was constructed using logic gates.

**OBJECTIVE 10.1: To design 3-bit ODD parity CHECKER:**

**THEORY:**

A parity check is the process that ensures accurate data transmission between nodes during communication and Parity checker is the combinational circuit to perform parity check.

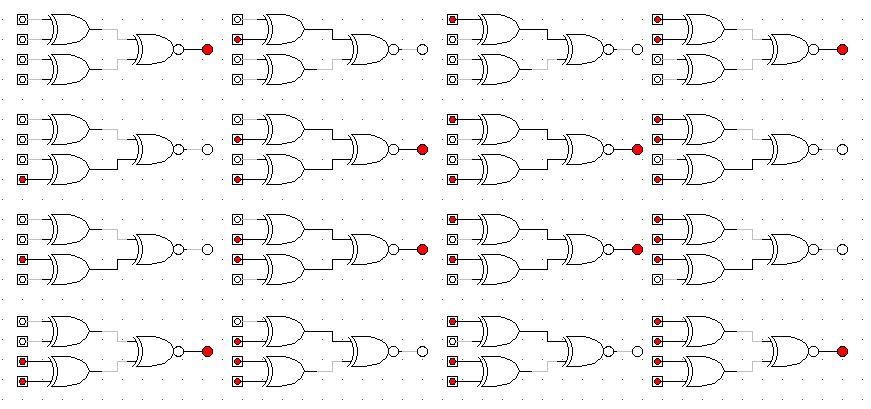
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Four bit received** | | | | **Parity error checker** |
| **x** | **y** | **z** | **p** | **c** |
| **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

**OBSERVATIONS:**

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**OBSERVATION TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Four bit received** | | | | **Parity error checker** |
| **x** | **y** | **z** | **p** | **c** |
| **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

**CONCLUSION:**

Hence, 3-bit odd parity checker was constructed using logic gates.

**OBJECTIVE 10.3:**

**To design 3-bit EVEN parity generator:**

**THEORY:**

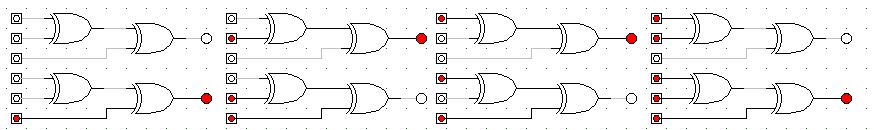
A Parity Generator is a Combinational Logic Circuit that Generates the Parity bit in the Transmitter. A Parity bit is used for the Purpose of Detecting Errors during Transmissions of binary Information. The total number of bits must be even in order to generate the even parity bit.

**CIRCUIT DIAGRAM:**

**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **3 bit message** | | | 3 Bit Parity Generated |
| **X** | **Y** | **Z** | **P** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**OBSERVATIONS:**

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**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **3 bit message** | | | 3 Bit Parity Generated |
| **X** | **Y** | **Z** | **P** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

**CONCLUSION:**

Hence, 3-bit even parity generator was constructed using logic gates.

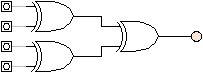
**OBJECTIVE 10.4:**

**To design 3-bit EVEN parity CHECKER:**

**THEORY:**

A parity check is the process that ensures accurate data transmission between nodes during communication and. Parity checker is the combinational circuit to perform parity check.

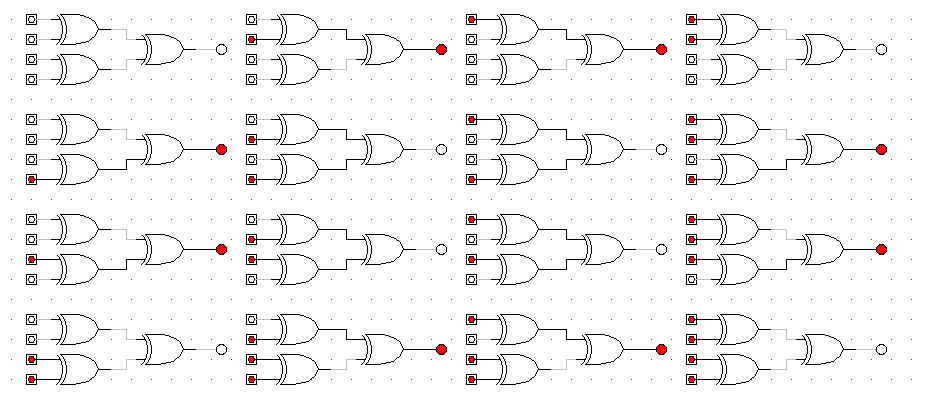
**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Four bit received** | | | | **Parity error checker** |
| **x** | **y** | **z** | **p** | **c** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **0** |

**OBSERVATIONS:**

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**OBSERVATION TABLE:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Four bit received** | | | | **Parity error checker** |
| **x** | **y** | **z** | **p** | **c** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **0** |

**CONCLUSION:**

Hence, 3-bit even parity checker was constructed using logic gates.